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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,328	LIN, CHANG-MING	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☒ Claim(s) *3-4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/749,328 filed on 12/29/2003.

2. Claims 1-27 have been submitted for examination.

3. Claims 1-27 have been examined.

Claim Objections

4. Claim 3-4 objected to because of the following informalities:

a. Regarding claim 3, the phrase "substantially simultaneously" renders the claim confusing. On page 8, paragraph 0028 of the specification, the applicant provides two examples of what is meant by substantially simultaneously. One of them is, "other suitably defined time period," which may be interpreted to be any time period. Two tasks could occur with the first completing multiple microseconds, or seconds, etc. before the second one starts and be considered substantially simultaneously, when it is a huge leap from being simultaneous in the computer world. Given a time period large enough, everything occurs substantially simultaneously

b. Claim 4 is objected to because of its dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claim 1-5, 20-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Beat, US Patent 6,912,173 and Brown, US Patent 6,434,657.

8. With respect to claim 1, Beat teaches of a method comprising: obtaining data to be written to a memory unit (fig. 1; column 3, lines 18-20);

determining if the data is aligned (fig. 7; column 8, lines 32-35), and

if the data is aligned, writing the data to memory (fig. 7; column 8, lines 35-37);

if the data is not aligned, writing the first portion of the first block to the second memory bank and the second portion of the first block to the first memory bank (fig. 1, 3b; 7; column 8, lines 38-51; where the even (2^{nd} portion) and odd (1^{st} portion) portions are written to the even (1^{st} memory bank) and odd memory (2^{nd} memory bank) sections).

Beat fails to explicitly teach of if the data is aligned, writing a first portion of a first block of the data to a first memory bank of the memory unit, and writing a second portion of the first block of the data to a second memory bank of the memory unit. However, Brown teaches of if the data is aligned, writing a first portion of a first block of the data to a first memory bank of the memory unit, and writing a second portion of the first block of the data to a second memory bank of the memory unit (fig. 4; column 3, lines 11-16; when the address is even (aligned), bits 0-9 (1^{st} portion) are written to block 0 (1^{st} memory bank) and bits 10-19 (2^{nd} portion) are written to block 1 (2^{nd} memory bank)).

Beat and Brown are analogous arts as they both write data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Beat and Brown at the time of the invention to write the 1^{st} data portion into the even memory section and the 2^{nd} data portion into the odd memory section in Beat as taught in Brown. Their motivation would have been to eliminate holes in the address space arising from writing word widths that are not a power of 2 times the read word width, Brown column 1, lines 22-37.

9. With respect to claim 2, Beat teaches of if the data is not aligned, writing the first portion of the first block to the second memory bank at a second address, and writing the second portion of the first block to the first memory bank at a third address (fig. 1, 3b, 7; column 3, lines 43-47; column 8, lines 38-51; where the even (2^{nd} portion) and odd (1^{st} portion) portions are written to the even (1^{st} memory bank) and odd memory

(2nd memory bank) sections; where the address for the odd memory bank is incrementally larger than the address for the even memory bank).

Beat fails to explicitly teach of if the data is aligned, writing the first portion of the first block to the first memory bank at a first address, and writing the second portion of the first block to the second memory bank at the first address. However, Brown teaches of if the data is aligned, writing the first portion of the first block to the first memory bank at a first address, and writing the second portion of the first block to the second memory bank at the first address (fig. 1, 4; column 3, lines 11-16; when the address is even (aligned), bits 0-9 (1st portion) are written to block 0 (1st memory bank) with WBL1 and bits 10-19 (2nd portion) are written to block 1 (2nd memory bank) with WBL1 in the same row).

10. With respect to claim 3, Beat teaches of in which the first portion and the second portion are written to the memory unit substantially simultaneously (column 3, lines 48-51; column 4, lines 11-15).

11. With respect to claim 4, Beat teaches of in which the first portion and the second portion are written to the memory unit on the same clock cycle (column 3, lines 48-51; column 4, lines 11-15; as the write operations occur simultaneously and in a single cycle; it is abundantly clear to one of ordinary skill of the art that they occur on the same clock cycle).

12. With respect to claim 5, Beat teaches of a system comprising: a data source (column 3, lines 18-22);

a data target, the data target including a memory unit, the memory unit including: a first memory bank; and a second memory bank (fig. 1; item 100; column 2, line 66-column 3, line 4);

logic for dividing the data into portions and accessing the first and second memory bank(fig. 1; items 110, 130; column 3, lines 52-58);

a bus communicatively connecting the data source and the data target, the bus being operable to transfer the first block of data from the data source to the data target (fig. 1; item 102; column 3, lines 18-22).

Beat fails to explicitly teach of logic for selecting data to be written to the first memory bank, the logic being operable to select a first portion of a first block of data if the first block of data is aligned, and to select a second portion of the first block of data if the first block of data is not aligned, and logic for selecting data to be written to the second memory bank, the logic being operable to select the first portion of the first block of data if the first block of data is not aligned, and to select the second portion of the first block of data if the first block of data is aligned;

However, Brown teaches of logic for selecting data to be written to the first memory bank, the logic being operable to select a first portion of a first block of data if the first block of data is aligned, and to select a second portion of the first block of data if the first block of data is not aligned (fig. 6; column 3, lines 44-65; when the data's address is even (aligned) the bits 1-9 (1^{st} portion) are selected for block 0, when the data's address is odd (not aligned) the bits 11-19 (2^{nd} portion) are selected for block 0);

logic for selecting data to be written to the second memory bank, the logic being operable to select the first portion of the first block of data if the first block of data is not aligned, and to select the second portion of the first block of data if the first block of data is aligned (fig. 6; column 3, lines 44-65; when the data's address is odd (not aligned) the bits 1-9 (1st portion) are selected for block 1, when the data's address is even (aligned) the bits 11-19 (2nd portion) are selected for block 1).

Beat and Brown are analogous arts as they both write data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Beat and Brown at the time of the invention to incorporate the address mapping circuit of Brown. Their motivation would have been to allow for the specific selection and direction of the different bit groups (Brown, column 1, lines 22-37).

13. With respect to claim 20, Beat teaches of a method for writing data to a memory unit, the method comprising: receiving a sequence of data blocks (fig. 1; column 3, lines 18-20);

obtaining a memory address at which to start writing the data blocks (fig. 1; column 3, lines 18-22)

determining whether the starting memory address is even or odd (fig. 7; column 8, lines 32-34; where it is determined if the data is aligned (even or odd address));

if the starting memory address is even, writing the data to memory (fig. 7; column 8, lines 34-37)

if the starting memory address is odd; writing the first portion of the first data block to the second memory bank at a location identified by a second address; writing

the second portion of the first data block to the first memory bank at a location identified by a third address (fig. 1, 3b, 7; column 3, lines 43-47; column 8, lines 40-51; where if the data is misaligned (odd address) the even (2nd portion) and odd (1st portion) portions are written to the even (1st memory bank) and odd memory (2nd memory bank) sections; where the address for the odd memory bank is incrementally larger than the address for the even memory bank).

Beat fails to explicitly teach of if the starting memory address is even; writing a first portion of a first data block in the sequence to a first memory bank at a location identified by a first address; writing a second portion of the first data block to a second memory bank at a location identified by the first address.

However, Brown teaches of if the starting memory address is even; writing a first portion of a first data block in the sequence to a first memory bank at a location identified by a first address; writing a second portion of the first data block to a second memory bank at a location identified by the first address (fig. 1, 4; column 3, lines 11-16; when the address is even, bits 0-9 (1st portion) are written to block 0 (1st memory bank) with WBL1 and bits 10-19 (2nd portion) are written to block 1 (2nd memory bank) with WBL1 in the same row).

Beat and Brown are analogous arts as they are both write data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Beat and Brown at the time of the invention to write the 1st data portion into the even memory section and the 2nd data portion into the odd memory section in Beat as taught in Brown. Their motivation would have been to eliminate holes in the address

space arising from writing word widths that are not a power of 2 times the read word width, Brown column 1, lines 22-37.

14. With respect to claim 21, the combination of Beat and Brown teach of the limitations previously cited with respect to claim 20. Additionally Beat and Brown both teach of the process repeating for other data (Beat, fig. 7; Brown, fig. 4). It is abundantly clear to one of ordinary skill in the art, that in storing additional data in memory, the data would be stored at an address other that the data recently stored so as not to overwrite the data just stored.

15. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Beat and Brown as applied to claim 5 above, and further in view of Melaragni et al., US Patent 6633576 (hereinafter Melaragni).

16. With respect to claim 6, the combination of Beat and Brown fails to explicitly teach of the data source comprises a microengine in a network processor.

However, Melaragni teaches of the data source comprises a microengine in a network processor (fig. 1, 2; column 4, lines 58-67; where the PDM (microengine) moves the data to a location in the memory. PDM is located within network processor 20).

The combination of Beat and Brown, and Melaragni are analogous arts as they both write data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Beat, Brown, and Melaragni at the time of the invention to include the network processor system of Melarangi around the memory system in the combination of Beat and Brown. Their motivation would have been to

allow a network user to receive data packets faster, sort and store packets in a memory and route them to their destination (Melaragni, column 4, lines 11-15).

17. Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Beat and Brown as applied to claim 5 above, and further in view of Wolrich et al., US Patent 6661794 (hereinafter Wolrich).

18. With respect to claim 7, the combination of Beat and Brown fails to explicitly teach of the data target comprises a scratchpad memory in a network processor.

However, Wolrich teaches of the data target comprises a scratchpad memory in a network processor (fig. 4; item 140; column 5, lines 14-16, lines 35-38; where the scratchpad memory in the network processor is accessed by the microengines and supports read and write operations).

The combination of Beat and Brown, and Wolrich are analogous arts as they both involve high speed memory access. It would have been obvious to one of ordinary skill in the art having the teachings of Beat, Brown, and Wolrich at the time of the invention to incorporate the scratchpad memory and the network processor containing it in Wolrich into the combination of Beat and Brown. Their motivation would have been to enable high speed processing of packet data, including packet forwarding (Wolrich, column 1, lines 14-16).

19. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Beat and Brown as applied to claim 5 above, and further in view of Wertheizer et al., US Patent 6,571,327 (hereinafter Wertheizer).

20. With respect to claim 8, the combination of Beat and Brown fails to explicitly teach of logic for selecting an address at which to write data to the first memory bank, the logic being operable to select a first address if the data is aligned, and to select a second address if the data is not aligned.

However, Wertheizer teaches of logic for selecting an address at which to write data to the first memory bank, the logic being operable to select a first address if the data is aligned, and to select a second address if the data is not aligned (fig. 5; column 7, lines 9-24; where muxes 72 and 74 are attached to the 1st and 2nd memory banks, respectively and select between two addresses depending on if the addresses are even or odd. If the initial address, I0, is even (data block is aligned), then I0 is selected by mux 72. In the case I0 is odd (data block is not aligned), I1 is selected by mux 72).

The combination of Beat and Brown, and Wertheizer are analogous arts as they both store data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Beat, Brown, and Wertheizer at the time of the invention to incorporate the address generation unit from Wertheizer into the address device of the combination of Beat and Brown. Their motivation would have been to provide an address for each of the memory banks from the input of a single address (Wertheizer, column 7, lines 9-24).

21. Claim 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Beat and Brown as applied to claim 20 above, and further in view of Tomita, US Patent Application 2002/0194420.

22. With respect to claim 22, the combination of Beat and Brown fails to explicitly teach of the first address is obtained by removing a bit from the starting address.

However, Tomita teaches of a first address is obtained by removing a bit from the starting address (paragraph 0007; where an address whose LSB is removed is supplied to the decoder of the even and odd memory array).

The combination of Beat and Brown, and Tomita are analogous arts as they both store data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Beat, Brown, and Tomita at the time of the invention to remove the LSB of the initial address when addressing the even and odd memory banks. Their motivation would have been to reduce the addressing overhead in addressing the even and odd memory banks since the LSB signifies such.

23. Claim 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Beat and Brown as applied to claim 20 above, and further in view of Cho, US Patent 6408040.

24. With respect to claim 23, the combination of Beat and Brown fails to explicitly teach of updating a count of the amount of data written to the memory unit; and if the count is less than a predefined value, writing additional data to the memory unit.

However, Cho teaches of updating a count of the amount of data written to the memory unit (fig. 11; item 1105, 1107; column 11, lines 13-22); and

if the count is less than a predefined value, writing additional data to the memory unit (fig. 11, 12; column 11, lines 27-55; if the data is not equal to 1536 bytes (predefined value), then it is invalid. If the invalid data is less than 1536 bytes, then dummy data is stored into the memory until it reaches 1536 bytes).

The combination of Beat and Brown, and Cho are analogous arts as they are both in the same field of endeavor, storing data into memory. It would have been obvious to one of ordinary skill in the art having the teachings of Beat, Brown, and Cho at the time of the invention to incorporate the process of ensuring valid data sizes. Their motivation would have been to avoid propagating prior data errors in processing the data (Cho, column 4, lines 28-46).

25. Claim 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Beat and Brown as applied to claim 20 above, and further in view of Burroughs et al., US Patent 6076136 (hereinafter Burroughs).

26. With respect to claim 24, the combination of Beat and Brown fails to explicitly teach of in which the blocks in the sequence comprise 64 bits, and in which the locations in the memory banks are 32 bits wide.

However, Burroughs teaches of in which the blocks in the sequence comprise 32 bits, and in which the locations in the memory banks are 16 bits wide (column 1, lines 18-23).

Furthermore, on page 10, in paragraph 33 of the applicant's specification, the applicant states, "it will be understood that the size of the various elements (e.g., 64-bit bus, 32-bit data blocks, 32-bit wide memory locations, etc.), and the relative proportions there between, have been chosen for the sake of illustration, and that the systems and methods described herein can be readily adapted to systems having components with different dimensions."

Additionally, it has been shown in In re Rose, 105 USPQ 237 and In re Rinehart 189 USPQ 143 that merely scaling or changing size is not patentably distinguishable.

The combination of Beat and Brown and Burroughs are analogous arts as they both store data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Beat, Brown and Burroughs at the time of the invention to make the data 3 or 64-bits and the memory banks 16 or 32-bits in the combination of Beat and Brown as taught in Burroughs in light of In re Rose and In re Rinehart as it is conventional (Burroughs, column 1, lines 18-23) and it has been held that merely scaling or changing size is not patentably distinguishable.

27. Claim 9-10, 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Wertheizer et al., US Patent 6,571,327 (hereinafter Wertheizer) and Brown et al., US Patent 4392201 (hereinafter Brown 2).

28. With respect to claim 9, Wertheizer teaches of a system comprising: a memory unit, the memory unit comprising: a first memory bank; and a second memory bank (fig. 3; items 2a, b; column 5, lines 31-37);

a third multiplexor, an output of the third multiplexor being communicatively coupled to an address input of the first memory bank, the third multiplexor being operable to select between a first address and a second address, the selection being based on whether the first data block is aligned, and to pass the selected address to the address input of the first memory bank (fig. 5; column 7, lines 9-24; where mux 72 and 74 are attached to the 1st and 2nd memory banks, respectively and select between two addresses depending on if the addresses are even or odd. If the initial address, I0, is

even (1st data block is aligned), then I0 is selected by mux 72. In the case I0 is odd (1st data block is not aligned), I1 is selected by mux 72).

Wertheizer fails to explicitly teach of a first multiplexor, an output of the first multiplexor being communicatively connected to the first memory bank, the first multiplexor being operable to select between a first portion of a first data block and a second portion of the first data block, the selection being based on whether the first data block is aligned, and to pass the selected portion to the first memory bank, and a second multiplexor, an output of the second multiplexor being communicatively connected to the second memory bank, the second multiplexor being operable to select between the first portion of the first data block and the second portion of the first data block, the selection being based on whether the first data block is aligned, and to pass the selected portion to the second memory bank.

However, Brown 2 teaches of a first multiplexor, an output of the first multiplexor being communicatively connected to the first memory bank, the first multiplexor being operable to select between a first portion of a first data block and a second portion of the first data block, the selection being based on whether the first data block is aligned, and to pass the selected portion to the first memory bank (fig. 19a; column 3, lines 13-50; column 47, line 46-column 47, line 15; the even mux selects the first data word if its address is even (1st data block aligned); and selects the second data word if it is odd (1st data block not aligned), as the second data word is addressed after the first and is addressed with an even address);

a second multiplexor, an output of the second multiplexor being communicatively connected to the second memory bank, the second multiplexor being operable to select between the first portion of the first data block and the second portion of the first data block, the selection being based on whether the first data block is aligned, and to pass the selected portion to the second memory bank (fig. 19a; column 3, lines 13-50; column 47, line 46-column 47, line 15; the odd mux selects the first data word if its address is odd (1st data block not aligned); and selects the second data word if it is even (1st data block aligned), as the second data word is addressed after the first and is addressed with an odd address);

Wertheizer and Brown 2 are analogous arts as they both store data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Wertheizer and Brown 2 at the time of the invention to incorporate the input selection muxes selecting a 1st or 2nd data portion from Brown 2 in Wertheizer. Their motivation would have been to supply the received data to the respective memory modules (Brown 2, column 3, lines 37-40).

29. With respect to claim 10, Wertheizer fails to explicitly teach of the first portion of the first data block comprises the least significant bits of the first data block, and in which the second portion of the first data block comprises the most significant bits of the first data block.

However, Brown 2 teaches of the first portion of the first data block comprises the least significant bits of the first data block, and in which the second portion of the first data block comprises the most significant bits of the first data block (fig. 19a; column 47,

lines 7-26, lines 46-50; where the 1st data word (portion) contains the LSBs: LDTR0:16 and the 2nd data word (portion) contains the MSBs: LDTR16:16. It is clear to one of ordinary skill in the art that the 2nd data word should read LDTR17:32, as the two 16-bit data words comprise a 32-bit block data).

30. With respect to claim 13, Wertheizer fails to explicitly teach of a bus having a width that is equal to the size of the first data block, the bus being operable to transfer the first data block from a master to the first and second multiplexors.

However, Brown 2 teaches of a bus having a width that is equal to the size of the first data block, the bus being operable to transfer the first data block from a master to the first and second multiplexors (fig. 19a; column 47, lines 7-9, 23-26, 46-50; where the local bus send to the input mux two 16 bit data words (a single data block), LBDT0:32. It is clear to one of ordinary skill in the art that the 32 bit data transmitted is the same size as the bus, as it is very inefficient to not use the full bus width in data transmission. It is also clear to one of ordinary skill in the art that there is some processing device (master) that has sent the data to the muxes).

31. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Wertheizer and Brown 2 as applied to claim 9 above, and further in view of Norman, US Patent application publication 2002/0004878.

32. With respect to claim 11, Wertheizer teaches of bank selection logic (fig. 3; item 48; column 4, lines 27-19).

The combination of Wertheizer and Brown 2 fails to explicitly teach of the bank select logic being operable to determine whether a first group of data has been written

to the first memory bank, and to at least temporarily disable the first memory bank from accepting additional data upon making said determination.

However, Norman teaches of bank select logic (fig. 3, 4; item 129), the bank select logic being operable to determine whether a first group of data has been written to the first memory bank (fig. 3, 4, 6; paragraph 0056; where the controller determines the updating data is identical to previously written data (a first group of data)), and

to at least temporarily disable the first memory bank from accepting additional data upon making said determination (fig. 3, 4, 6; paragraph 0056; where the controller prevented a write of the updating data to the array (first memory bank) after determining it is identical to previously written data).

The combination of Wertheizer and Brown 2, and Norman are analogous arts as they are both in the same field of endeavor, accessing data in memory. It would have been obvious to one of ordinary skill in the art having the teachings of Wertheizer, Brown 2, and Norman at the time of the invention to include the ability to prevent writing to the array when the to be data written is identical to data already stored. Their motivation would have been to increase efficiency by avoiding redundant write operations (paragraph 0036, 0038).

33. Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Wertheizer and Brown 2 as applied to claim 9 above, and further in view of Roth et al., US Patent 4720783.

34. With respect to claim 12, the combination of Weretheizer and Brown 2 fails to explicitly teach of a FIFO memory operable to store the first data block, the FIFO

memory being communicatively coupled to a bus and operable to accept incoming blocks of data from the bus, the FIFO memory being further communicatively coupled to the first and second multiplexors.

However Roth teaches of a FIFO memory operable to store a first data block, the FIFO memory being communicatively coupled to a bus and operable to accept incoming blocks of data from the bus, a FIFO memory being further communicatively coupled to a multiplexor (fig. 1; column 5, lines 6-30; where the FIFO is connected to the host CPU by a bus, and is connected to a mux. It is abundantly clear to one of ordinary skill in the art that the FIFO buffer is able to store a first data block).

The combination of Weretheizer and Brown 2, and Roth are analogous arts as they both transfer digital data. It would have been obvious to one of ordinary skill in the art having the teachings of Weretheizer, Brown 2, and Roth at the time of the invention to include the FIFO buffer from Roth inline before the cache data input muxes of the combination of Weretheizer and Brown 2. Their motivation would have been to enable buffering of the input data to compensate for momentary delays that may occur while receiving the data.

35. Claim 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Wertheizer and Brown 2 as applied to claim 13 above, and further in view of admitted prior art by the applicant.

36. With respect to claim 14, the combination of Wertheizer and Brown 2 fails to explicitly teach of the master is designed to process blocks of data that are half the width of the first data block.

However, the applicant's prior art admission teaches of the master is designed to process blocks of data that are half the width of the first data block (specification, page 1; paragraph 0004; where a processor (master) operates on 32-bit blocks and the transported data block is 64 bits).

It would have been obvious to one of ordinary skill in the art having the teachings of Wertheizer, Brown 2 and the applicant's prior art admission at the time of the invention to make the processing device in the combination of Wertheizer and Brown 2 able to process blocks half the size of the local bus. Their motivation would have been to conserve money and space on the circuit board by using a smaller processor that doesn't need pin outs for the entire bus width.

37. Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Wertheizer and Brown 2 as applied to claim 13 above, and further in view of Sugita, US patent 5659711.

38. With respect to claim 15, the combination of Wertheizer and Brown 2 fails to explicitly teach of the first memory bank is half the width of the first data block, and in which the second memory bank is half the width of the first data block.

However, Sugita teaches of the first memory bank is half the width of the first data block, and in which the second memory bank is half the width of the first data block (fig. 9; column 4, lines 34-46).

The combination of Wertheizer and Brown 2, and Sugita are analogous arts as they both are related to memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of Wertheizer, Brown 2 and Sugita at the

time of the invention to make the width of the memory banks half that of the width of the data word in the combination of Wertheizer and Brown 2 as taught in Sugita. Their motivation would have been to provide for efficient use of the memory.

39. Claim 16 and 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Wertheizer and Brown 2 as applied to claim 9 above, and further in view of admitted prior art by the applicant.

40. With respect to claim 16, the combination of Wertheizer and Brown 2 fails to explicitly teach of the first data block is 64-bits long.

However, the applicant's admitted prior art teaches of the first data block is 64-bits long (specification, page 1; paragraph 0004).

It would have been obvious to one of ordinary skill in the art having the teachings of Wertheizer, Brown 2 and the applicant's prior art admission at the time of the invention to make the data block size 64 bits in the combination of Wertheizer and Brown 2 to increase the amount of data transferred.

41. With respect to claim 17, the combination of Wertheizer and Brown 2 teaches of transferring the data from a master to the first and second multiplexors (as cited previously). The combination of Wertheizer and Brown 2 fails to explicitly teach of a 64-bit bus, the 64-bit bus being operable to transfer the first data block from a 32-bit master.

However, the applicant's prior art admission teaches of a 64-bit bus, the 64-bit bus being operable to transfer the first data block from a 32-bit master (specification, page 1; paragraph 0004).

It would have been obvious to one of ordinary skill in the art having the teachings of Wertheizer, Brown 2 and the applicant's prior art admission at the time of the invention to make the processing device 32-bit and the data bus 64-bit in the combination of Wertheizer and Brown 2 to conserve money and space on the circuit board by using a smaller processor that doesn't need pin outs for the entire bus width..

42. Claim 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Wertheizer and Brown 2 and applicant's prior art admission as applied to claim 17 above, and further in view of Melaragni.

43. With respect to claim 18, the combination of Wertheizer, Brown 2 and applicant's prior art admission teach of a 32-bit master (as cited with respect to claim 17). The combination of Wertheizer, Brown 2 and applicant's prior art admission fails to specifically teach of the master being a microengine in a network processor.

However, Melaragni teaches of a master comprising a microengine in a network processor (fig. 1, 2; column 4, lines 58-67; where the PDM (microengine) moves the data to a location in the memory. PDM is located within network processor 20).

The combination of Wertheizer, Brown 2 and applicant's prior art admission, and Melaragni are analogous arts as they both write data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Wertheizer, Brown 2, applicant's prior art admission, and Melaragni at the time of the invention to include the network processor system of Melarangi around the memory system in the combination of Wertheizer, Brown 2 and applicant's prior art admission. Their motivation would have been to allow a network user to receive data packets

faster, sort and store packets in a memory and route them to their destination (Melaragni, column 4, lines 11-15).

44. Claim 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Wertheizer, Brown 2, applicant's prior art admission, and Melaragni as applied to claim 18 above, and further in view of Wolrich.

45. With respect to claim 19, the combination of Wertheizer, Brown 2, applicant's prior art admission, and Melaragni, fails to explicitly teach of the memory unit comprises a scratchpad memory in the network processor.

However, Wolrich teaches of a memory unit comprises a scratchpad memory in the network processor (fig. 4; item 140; column 5, lines 14-16, lines 35-38; where the scratchpad memory in the network processor is accessed by the microengines and supports read and write operations).

The combination of Wertheizer, Brown 2, applicant's prior art admission, and Melaragni and Wolrich are analogous arts as they both involve high speed memory access. It would have been obvious to one of ordinary skill in the art having the teachings of Wertheizer, Brown 2, applicant's prior art admission, Melaragni, and Wolrich at the time of the invention to incorporate the scratchpad memory in Wolrich into the memory in the combination of Wertheizer, Brown 2, applicant's prior art admission, and Melaragni. Their motivation would have been to enable high speed processing of packet data, including packet forwarding (Wolrich, column 1, lines 14-16).

46. Claim 25, 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Beat, Brown, and Wybenga et al., US patent application 2004/0223502 (hereinafter Wybenga).

47. With respect to claim 25, Beat and Brown teach of all the limitations previously cited with respect to claim 5. Beat and Brown fail to explicitly teach of a first line card, the first line card comprising: one or more physical layer devices; one or more framing devices; and one or more network processors, at least one network processor comprising: a microengine.

However, Wybenga teaches of a first line card (fig. 1; item 110, 123, 130, 140; paragraph 0024), the first line card comprising: one or more physical layer devices (fig. 1, 2; item 112, 114; paragraph 0024-0025; where each routing node contains one or more physical medium devices (PMD)); one or more framing devices (fig. 1, 2; item 112, 114; paragraph 0024-0025; where the PMD modules also frames an incoming packet); and one or more network processors (fig. 2; item 260; paragraph 0029), at least one network processor comprising: a microengine (fig. 2; paragraph 0029; where the network processor comprises microengines).

Beat and Brown are analogous arts as they both write data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Beat and Brown at the time of the invention to incorporate the address mapping circuit of Brown. Their motivation would have been to allow for the specific selection and direction of the different bit groups (Brown, column 1, lines 22-37).

The combination of Beat and Brown, and Wybenga are analogous arts as they are both in the same field of endeavor, data manipulation. It would have been obvious to one of ordinary skill in the art having the teachings of Beat, Brown, and Wybenga at the time of the invention to incorporate the distributed architecture router, including the network processor around the memory system in the combination of Beat and Brown. Their motivation would have been to have a parallel distributed architecture router that does not require a dedicated forwarding table for each type of IP data traffic (Wybenga, paragraph 0007).

48. With respect to claim 27, Wybenga teaches of a second line card; and a switch fabric operable to communicatively couple the first line card and the second line card (fig. 1; item 120, 150; paragraph 0024).

49. Claim 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Beat, Brown, and Wybenga as applied to claim 25 above, and further in view of Wertheizer.

50. With respect to claim 26, the combination of Beat, Brown, and Wybenga fails to explicitly teach of logic for selecting an address at which to write data to the first memory bank, the logic being operable to select a first address if the data is aligned, and to select a second address if the data is not aligned.

However, Wertheizer teaches of logic for selecting an address at which to write data to the first memory bank, the logic being operable to select a first address if the data is aligned, and to select a second address if the data is not aligned (fig. 5; column 7, lines 9-24; where muxes 72 and 74 are attached to the 1st and 2nd memory banks, respectively and select between two addresses depending on if the addresses are even or odd. If the

initial address, I0, is even (data block is aligned), then I0 is selected by mux 72. In the case I0 is odd (data block is not aligned), I1 is selected by mux 72).

The combination of Beat, Brown, and Wybenga and Wertheizer are analogous arts as they both store data into even and odd memory banks. It would have been obvious to one of ordinary skill in the art having the teachings of Beat, Brown, Wybenga, and Wertheizer at the time of the invention to incorporate the address generation unit from Wertheizer into the address device of the combination of Beat, Brown, and Wybenga. Their motivation would have been to provide an address for each of the memory banks from the input of a single address (Wertheizer, column 7, lines 9-24).

Conclusion

51. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

52. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

53. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

54. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW D. ANDERSON
PRIMARY EXAMINER